

### ■ Description

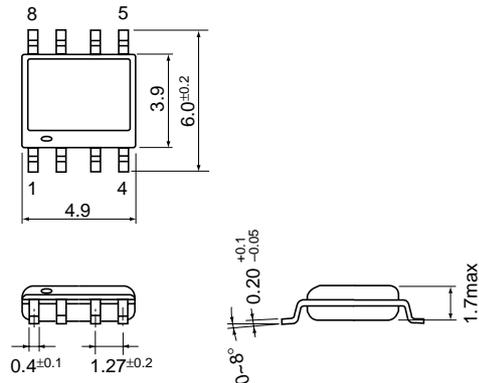
The FA3641P(N) and FA3647P(N) are the PWM type switching power supply control ICs that can directly drive power MOSFET. These ICs use a CMOS device with high dielectric strength (30V) to implement low power consumption. They feature a number of functions that are equivalent to those of the FA531X series consisting of bipolar devices. In addition, they have a function that reduces the oscillation frequency to suppress loss of the power supply in light load mode and support an overvoltage protection detecting  $V_{cc}$  voltage. These ICs are most suitable for high-performance, energy-saving power supplies that require low input power in standby or no-load mode.

### ■ Features

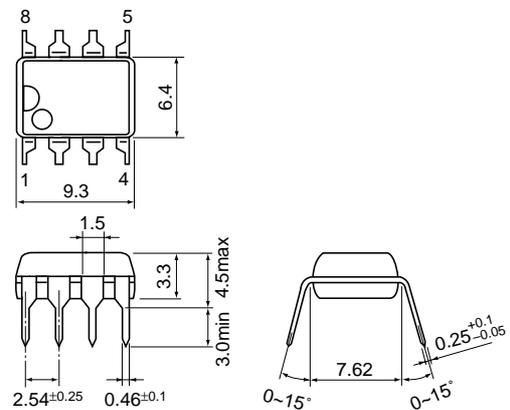
- Uses a newly developed CMOS process with high dielectric strength (30V) for implementing low power consumption
- Standby current of  $2\mu\text{A}$  or less (at  $V_{cc}=14\text{V}$ ), and operating current of  $1.9\text{mA}$  (typ.)
- Automatically reduces the oscillation frequency to suppress loss of the power supply in light load mode
- Overvoltage protection function detecting  $V_{cc}$  voltage
- A drive circuit for connecting a power MOSFET directly
- Output peak current: Source current  $-500\text{mA}$   
Sink current  $+1\text{A}$
- Pulse-by-pulse overcurrent limiting function
- Overload cutoff function (latch or non-latch mode selectable)
- Output ON/OFF control function by external signal
- Latch mode overvoltage shutdown function
- Undervoltage lockout function (16.5V ON / 9V OFF)
- Reference voltage output (5V)
- 8-pin package (DIP/SOP)

### ■ Dimensions, mm

#### ● SOP-8

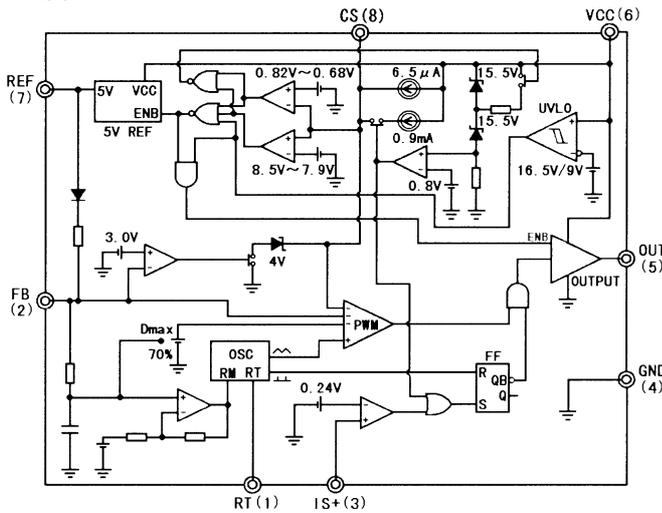


#### ● DIP-8

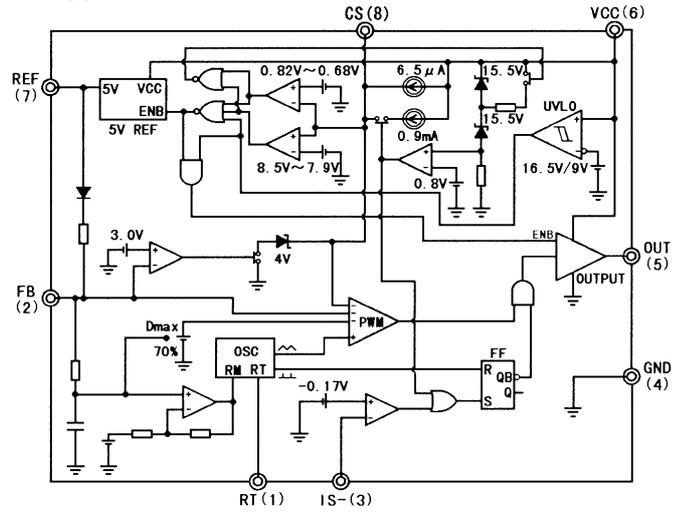


■ Block diagram

● FA3641



● FA3647



Pin No.	Symbol	Function	Description
1	RT	Oscillator timing resistor	Setting oscillation frequency
2	FB	Feedback	Input to PWM comparator
3	IS (+)/ IS (-)	Overcurrent detection	Input to overcurrent limiting function
4	GND	Ground	Ground
5	OUT	Output	Output for direct driving a power MOSFET
6	VCC	Power supply	Power supply for IC
7	REF	Reference voltage	Reference voltage output (5V)
8	CS	Soft-start and ON/OFF control	Soft-start, ON/OFF and latch-mode shutdown operations

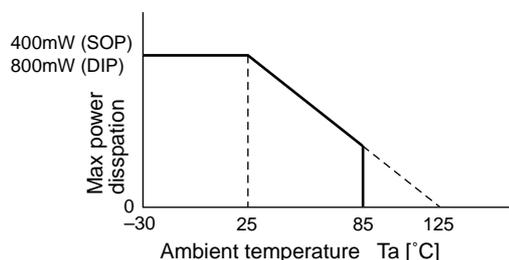
■ Absolute maximum ratings (Ta=25°C)

Item	Symbol	Test condition	Rating	Unit
Supply voltage	Vcc1	Low impedance source (Icc > 15mA)	30	V
	Vcc2	Internal ZD clamp (Icc < 15mA)	Self limiting	V
Output peak current	IoL	Sink current	+1.0	A
	IoH	Source current	-0.5	A
FB pin input voltage	VFB		-0.3 to 5.0	V
REF pin output current	IREF		-10	mA
IS pin input voltage	Vis		-0.3 to 5.0	V
CS pin input current	Ics		2.0	mA
Total power dissipation	Pd	at Ta =25°C DIP	800 *1	mW
		SOP	400 *2	
Operating temperature	Topr		-30 to +85	°C
Junction temperature	Tj		125	°C
Storage temperature	Tstg		-40 to +150	°C

Note: \*1 Derating factor Ta > 25°C: 8.0mW/°C

\*2 Derating factor Ta > 25°C: 4.0mW/°C

Maximum power dissipation curve



## FA3641P(N), FA3647P(N)

### ■ Recommended operating condition

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>CC</sub>	10		28	V
REF pin bypass capacitor	C <sub>ref</sub>	0.1	0.47		μF
Soft-start capacitor	C <sub>s</sub>	0.01		1	μF
Oscillation frequency (FB >1.2V)	f <sub>osc</sub>	30		500	kHz
Min. oscillation frequency at light load mode (FB <1.2V)	f <sub>oscL</sub>	10			kHz

### ■ Electrical characteristics (V<sub>CC</sub>=18V, R<sub>T</sub>=47kΩ, T<sub>a</sub>=25°C)

#### Reference voltage section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Reference voltage	V <sub>REF</sub>	T <sub>j</sub> =25°C	4.75	5.00	5.25	V
Voltage variation 1 (Line regulation)	V <sub>dV</sub>	V <sub>CC</sub> =10 to 28V		±6	±20	mV
Voltage variation 2 (Load regulation)	V <sub>dV</sub>	I <sub>L</sub> =0 to 10mA, V <sub>CC</sub> =18V		±6	±20	mV
Voltage variation 3 (Temperature stability)	V <sub>dT</sub>	T <sub>a</sub> = -30 to +85°C		±0.5		mV/°C

#### Oscillator section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f <sub>osc</sub>	R <sub>T</sub> =47kΩ, T <sub>j</sub> =25°C	92.6	100	107.4	kHz
Frequency variation 1 (Voltage stability)	f <sub>dV</sub>	V <sub>CC</sub> =10 to 28V		±1.6		%
Frequency variation 2 (Temperature stability)	f <sub>dT</sub>	T <sub>a</sub> = -30 to +85°C		±0.02		% / °C

#### Pulse width modulation circuit section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
FB pin source current	I <sub>FB</sub>	V <sub>FB</sub> =0V	-985	-750	-615	μA
Input threshold voltage (FB pin)	V <sub>TH FBO</sub>	Duty cycle =0%	0.95	1.03		V
	V <sub>TH FBM</sub>	Duty cycle =D <sub>MAX</sub>		2.40		V
Maximum duty cycle	D <sub>MAX</sub>	V <sub>FB</sub> =2.5V	66	70	74	%

#### Reducing oscillation frequency section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
FB pin threshold voltage	V <sub>TH FBS</sub>			1.18		V
Frequency reduction	k <sub>FS1</sub>	V <sub>FB</sub> =1.10 to 1.15V		16.7		kHz
Minimum oscillation frequency	f <sub>oscS2</sub>			46		kHz

#### Overcurrent limiting circuit section

Item	Symbol	Test condition	FA3641P/N			FA3647P/N			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input threshold voltage (IS pin)	V <sub>TH IS</sub>		215	235	255	-188	-168	-148	mV
Input terminal source current (IS pin)	I <sub>IS</sub>	V <sub>IS</sub> =0V			-5		-20		μA
Delay time	T <sub>PD IS</sub>			150			150		ns

#### Soft-start circuit section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Charge current (CS pin)	I <sub>CHG</sub>	V <sub>CS</sub> =1V, T <sub>j</sub> =25°C	-4.0	-6.5	-9.0	μA
Input threshold voltage (CS pin)	V <sub>TH CSO</sub>	Duty cycle =0%	0.95	1.03		V
	V <sub>TH CSM</sub>	Duty cycle =D <sub>MAX</sub>		2.40		V

**Output ON/OFF circuit section**

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
CS pin <sub>1</sub> source current	Isocs	Vcs=0V, Tj=25°C	-4.0	-6.5	-9.0	μA
OFF-to-ON threshold voltage (CS pin)	V <sub>TH ON</sub>	OFF→ON, Tj=25°C		0.82	0.95	V
ON-to-OFF threshold voltage (CS pin)	V <sub>TH OFF</sub>	ON→OFF, Tj=25°C	0.50	0.68		V

**Latch-mode cutoff circuit section**

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
CS pin sink current	ISICS	Vcs=6.5V, VFB=1V, Tj=25°C	20	35	50	μA
Cutoff threshold voltage (CS pin)	V <sub>TH CSF</sub>	ON→OFF, Tj=25°C	8.0	8.5	9.0	V
	V <sub>TH CSN</sub>	OFF→ON, Tj=25°C	7.4	7.9	8.4	V
Hysteresis	V <sub>TH HIS</sub>			0.6		V

**Overload cutoff circuit section**

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Cutoff threshold voltage (FB pin)	V <sub>TH FB</sub>		2.8	3.0	3.3	V

**Overvoltage cutoff circuit section**

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Cutoff threshold voltage (Vcc pin)	V <sub>TH VCC</sub>	Tj=25°C	30	32	34	V
Cutoff operating supply current (Vcc pin)	I <sub>VCC</sub>	Tj=25°C		13		mA
Charge current (CS pin)	ISO CS2	Vcs=6.5V	-0.5	-0.9	-1.4	mA

**Undervoltage lockout circuit section**

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
OFF-to-ON threshold voltage	V <sub>CC ON</sub>	Tj=25°C	15.5	16.5	17.5	V
ON-to-OFF threshold voltage	V <sub>CC OFF</sub>	Tj=25°C	8.5	9.0	10.0	V
Hysteresis	V <sub>HYS</sub>	Tj=25°C	6.8	7.5	8.2	V

**Output section**

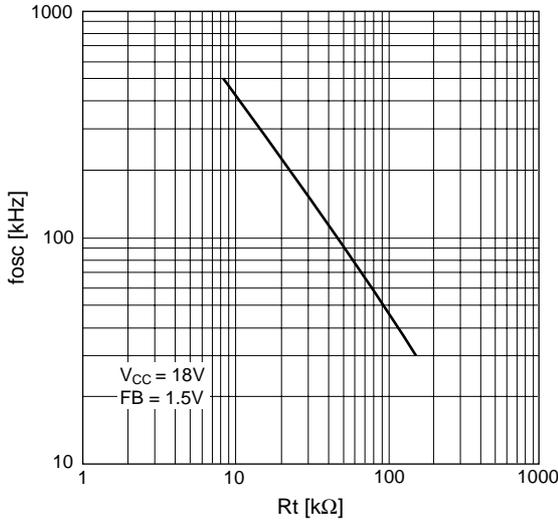
Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
L-level output Voltage	V <sub>OL</sub>	I <sub>O</sub> =100mA		0.7	1.5	V
H-level output Voltage	V <sub>OH</sub>	I <sub>O</sub> =-100mA, Vcc=18V	15	16.5		V
Rise time	tr	OUT=1000pF		50		ns
Fall time	tf	OUT=1000pF		40		ns

**Overall device**

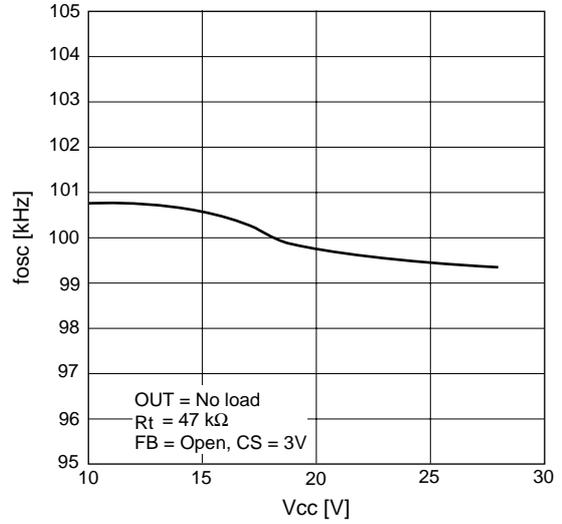
Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Standby current	I <sub>CC STB</sub>	Vcc=14V			2	μA
Startup current	I <sub>CC ST</sub>	Vcc=VccON		12	30	μA
Operating-state supply current	I <sub>CC OP</sub>	No load		1.9	2.5	mA
OFF-state supply current	I <sub>CC OF</sub>	Vcc=17V, Cs=0V		100		μA
Cutoff-state supply current	I <sub>CC L</sub>	Vcc=10V		45	100	μA

■ Characteristic curves (Ta=25°C)

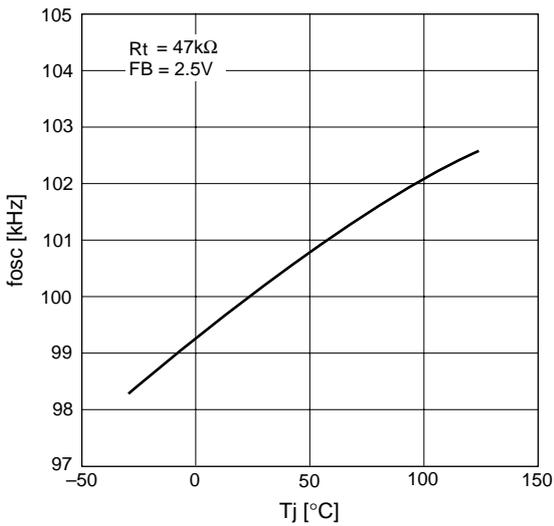
Oscillation frequency (fosc) vs. timing resistor resistance (Rt)



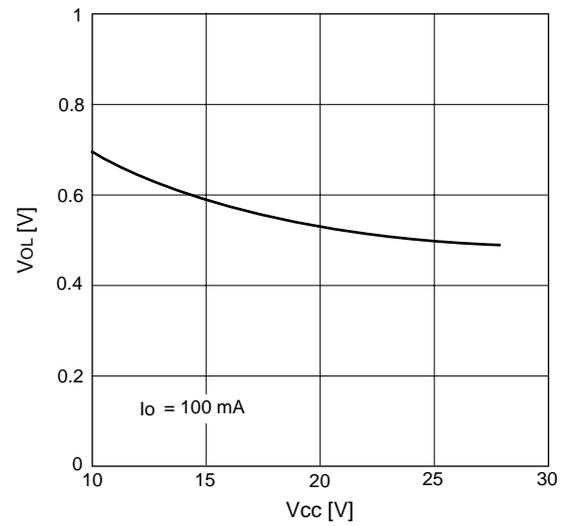
Oscillation frequency (fosc) vs. supply voltage (Vcc)



Oscillation frequency (fosc) vs. junction temperature (Tj)

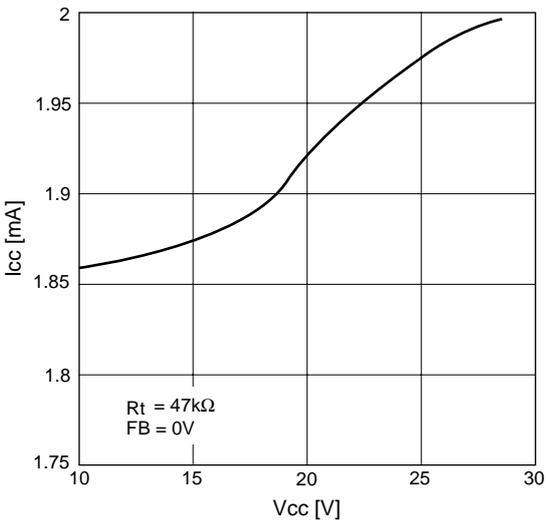


L-level output vltage (VoL) vs. supply voltage (Vcc)



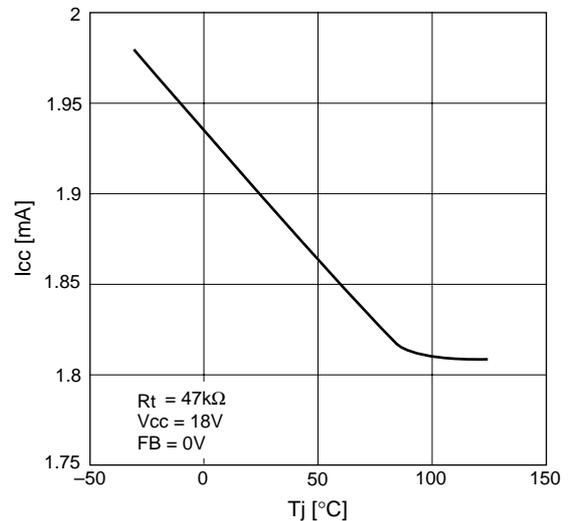
Supply current (Icc) vs. supply voltage (Vcc)

Operating mode



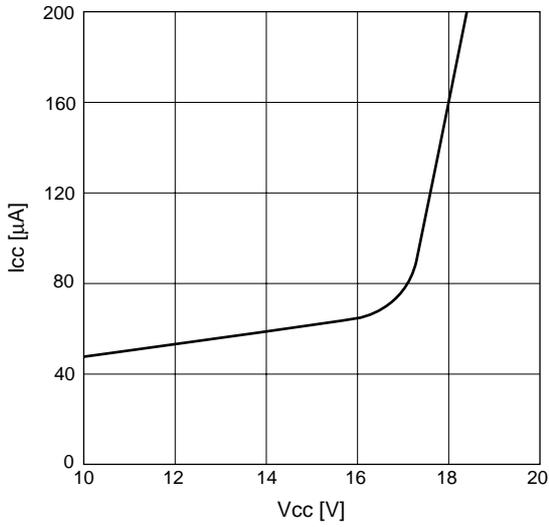
Supply current (Icc) vs. junction temperature (Tj)

Operating mode



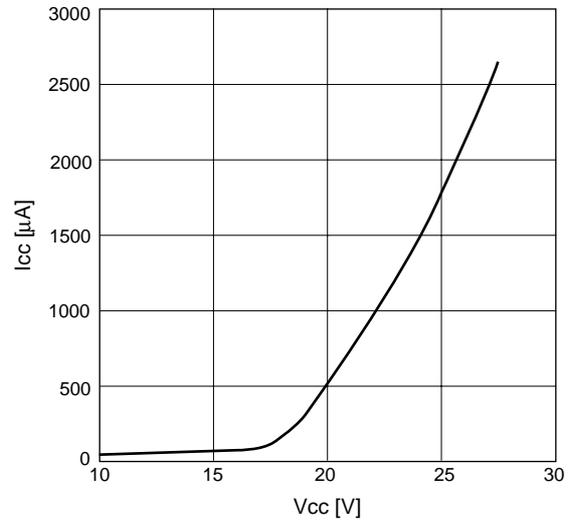
Supply current ( $I_{CC}$ ) vs. supply voltage ( $V_{CC}$ )

Latch mode



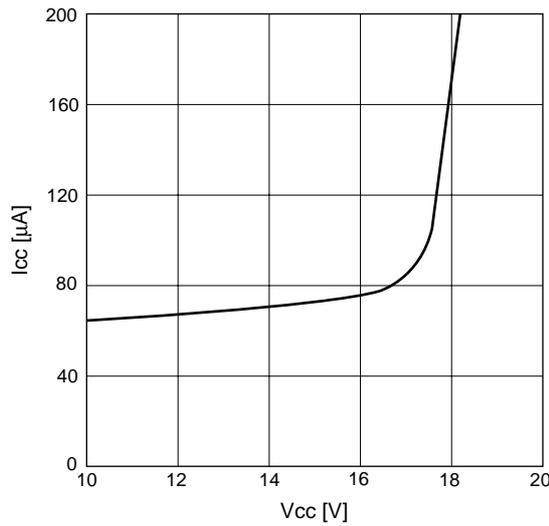
Supply current ( $I_{CC}$ ) vs. supply voltage ( $V_{CC}$ )

Latch mode



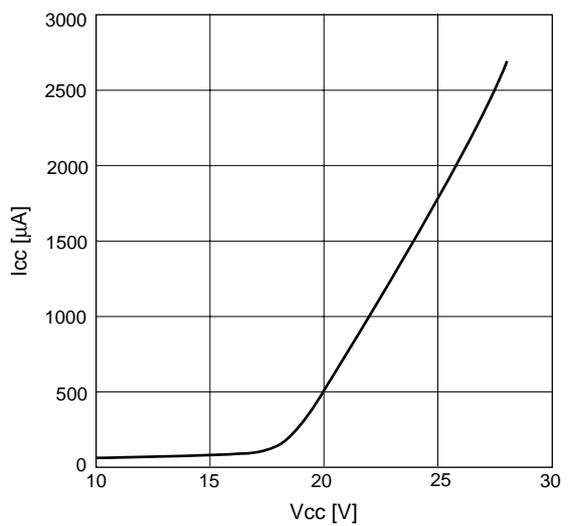
Supply current ( $I_{CC}$ ) vs. supply voltage ( $V_{CC}$ )

OFF mode

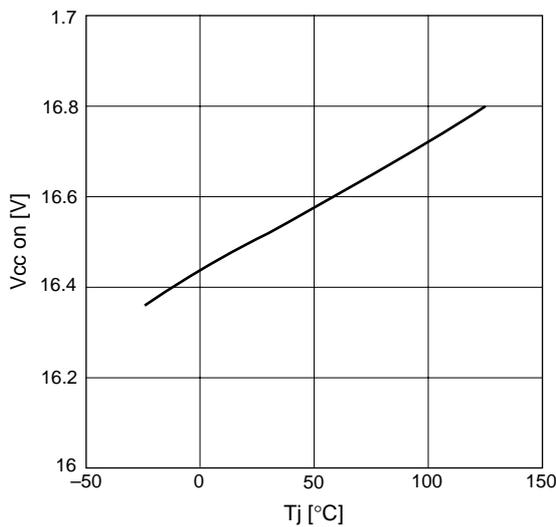


Supply current ( $I_{CC}$ ) vs. supply voltage ( $V_{CC}$ )

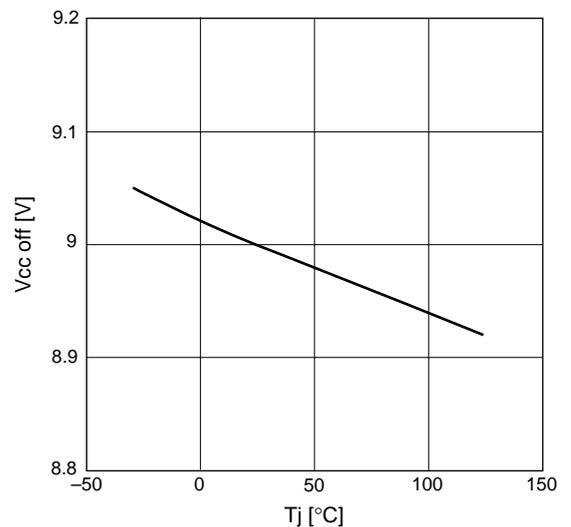
OFF mode



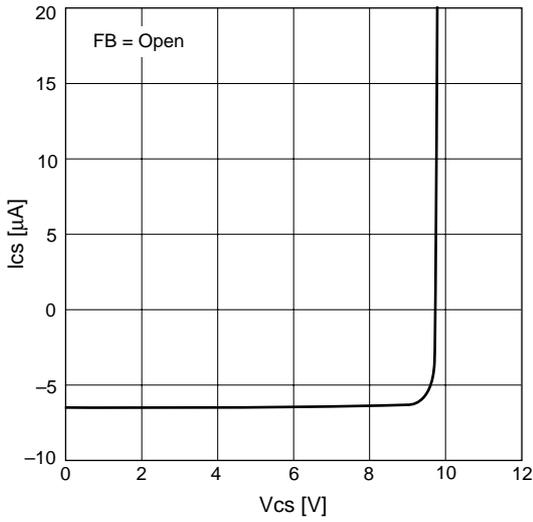
UVLO OFF-to-ON threshold voltage ( $V_{CC\ on}$ ) vs. junction temperature ( $T_j$ )



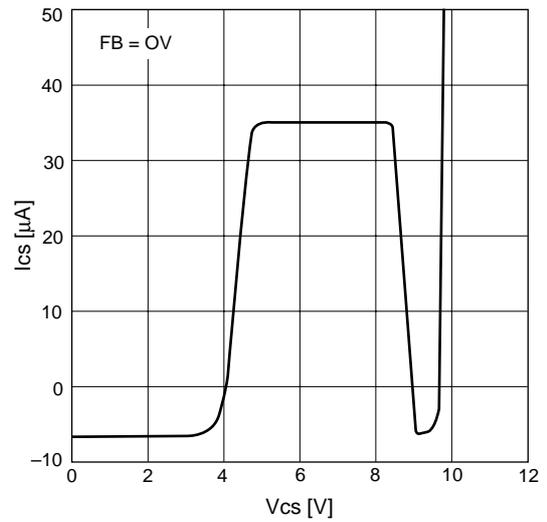
UVLO ON-to-OFF threshold voltage ( $V_{CC\ off}$ ) vs. junction temperature ( $T_j$ )



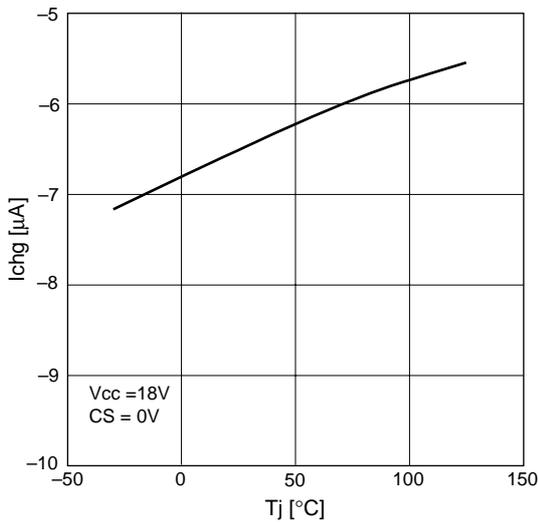
CS terminal current ( $I_{CS}$ ) vs. CS terminal voltage ( $V_{CS}$ )



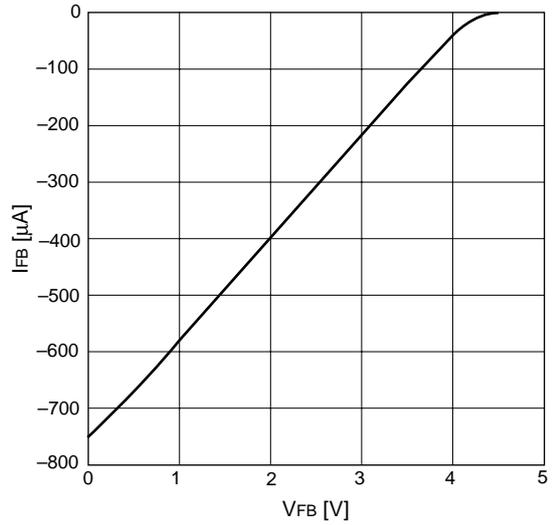
CS terminal current ( $I_{CS}$ ) vs. CS terminal voltage ( $V_{CS}$ )



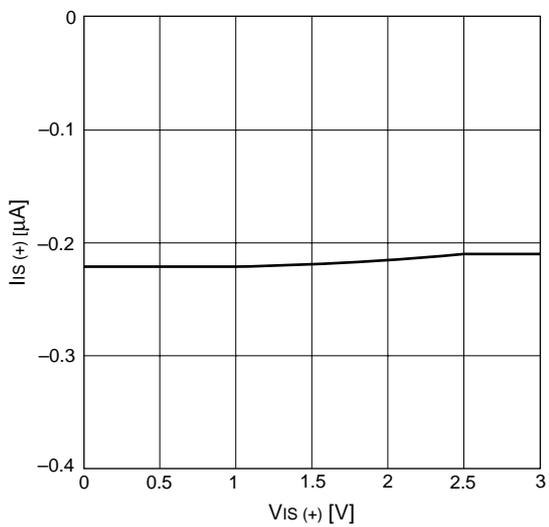
CS terminal charge current ( $I_{chg}$ ) vs. junction temperature ( $T_j$ )



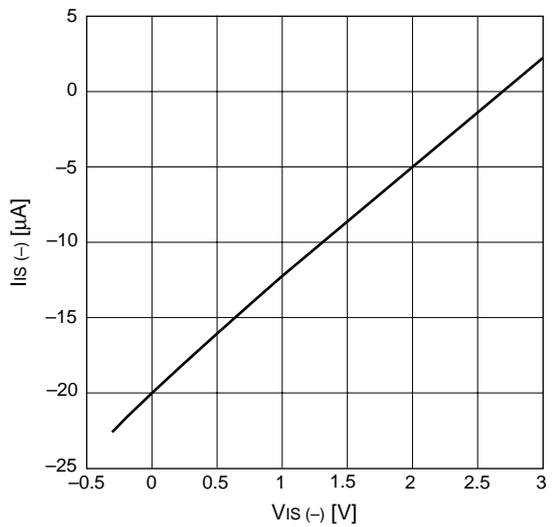
FB terminal source current ( $I_{FB}$ ) vs. FB terminal voltage ( $V_{FB}$ )



IS (+) terminal current ( $I_{IS (+)}$ ) vs. IS (+) terminal voltage ( $V_{IS (+)}$ )  
FA3641



IS (-) terminal current ( $I_{IS (-)}$ ) vs. IS (-) terminal voltage ( $V_{IS (-)}$ )  
FA3647



■ Description of each circuit

1. Oscillator

The oscillator generates a triangular waveform by charging and discharging the built-in capacitor. A desired oscillation frequency can be set by the value of the resistor connected to the RT pin (See Figure 1).

The built-in capacitor voltage oscillates between about 3V and 1V, with almost the same charging and discharging gradients (Figure 2). You can set the desired oscillation frequency by changing the gradients using the resistor connected to the RT pin. (Large  $R_t$  = low frequency, small  $R_t$  = high frequency) The oscillation frequency is automatically lowered when output duty cycle is small ( $FB \leq$  about 1.18V) in light load mode. For more information, see item 2, "Reducing oscillation frequency circuit in light-load mode."

The relationship between  $R_t$  and the fixed oscillation frequency is approximately given by:

$$f_o \text{ [kHz]} \approx \frac{4880}{R_t + 1.4} \dots\dots\dots (1)$$

$$R_t \text{ [k}\Omega] \approx \frac{4880}{f_o} - 1.4 \dots\dots\dots (2)$$

$f_o$ : Fixed frequency [kHz]

$R_t$ : Timing resistance [k $\Omega$ ]

The oscillator waveform cannot be observed from the outside because a pin for this purpose is not provided. The oscillator output is connected to a PWM comparator. The RT pin is 2.5V DC in normal fixed frequency operation mode. When the frequency is lowered, the voltage also decreases linearly to about 1V.

2. Reducing oscillation frequency circuit in light-load mode

To reduce the loss of the power supply in standby mode, this IC has a feature that automatically lowers the oscillation frequency when the load is light. When the load is light, with the result that the IC output pulse width narrows below about 10% and the FB pin voltage decreases below about 1.18V, the oscillation frequency begins to decrease linearly until the output pulse width becomes 0. When the output pulse width is 0, the oscillation frequency is about 46% of normal fixed frequency (Figure 3). Even while the oscillation frequency is decreasing, the built-in capacitor voltage oscillates between about 3V and 1V.

The frequency reduction rate (46%) can be adjusted from the outside. (See "Design advice" for more information.)

3. PWM comparator

The PWM comparator has four inputs as shown in Figure 4. Oscillator output ① is compared with CS pin voltage ②, FB pin voltage ③, and DT voltage ④. The lowest of three inputs ②, ③, and ④ has priority and is compared with output ①. While the voltage is lower than the oscillator output, the comparator output is high. While the voltage is higher than the oscillator output, the PWM comparator output is low (see Figure 5). The IC OUT pin voltage is high while the PWM comparator output is low.

When the IC is powered up, CS pin voltage ② controls soft start operation. The output pulse then begins to widen gradually. During normal operation, the output pulse width is determined within the maximum duty cycle (70%) set by DT voltage ④ under the condition set by FB pin voltage ③, to stabilize the output voltage.

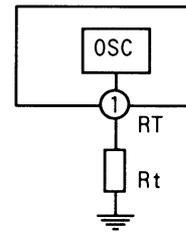


Fig. 1 Oscillator

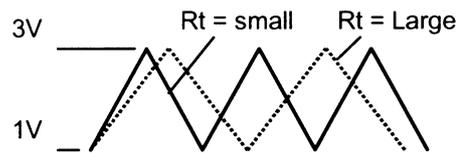


Fig. 2 Oscillator output

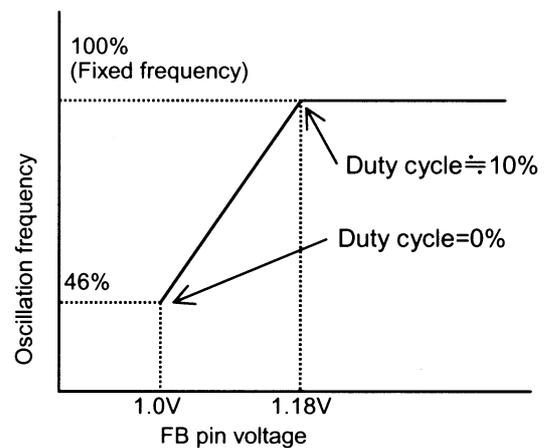


Fig. 3 Oscillation frequency

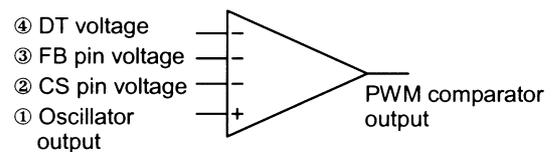


Fig. 4 PWM comparator

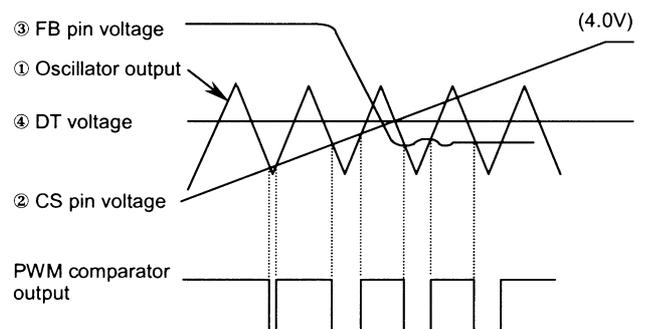


Fig. 5 PWM comparator timing chart

**4. CS pin circuit**

As shown in Figure 6, capacitor Cs is connected to the CS pin. The CS pin voltage varies depending on the charging voltage of this capacitor Cs. When the power is turned on, the constant current source (6.5µA) begins to charge capacitor. Accordingly, the CS pin voltage rises as shown in Figure 7. The CS pin voltage is connected to the PWM comparator, which is characterized to make output based on the lowest of input voltages. The device enters soft-start mode while the CS pin voltage is between 1.0V and 2.4V. During normal operation, the CS pin is clamped at 4.0V by internal zener diode.

If the output voltage drops due to an overload and the FB voltage rises to 3V or more, the clamp voltage 4.0V is canceled and the CS pin voltage rises to 9.5V. The CS pin is also connected to latch comparator C2. If the CS pin voltage rises to 8.5V or more, comparator C2 toggles to turn off the 5V REF circuit, thereby shutting the output down. Since the CS pin is also connected to comparator C1, the 5V REF circuit can be turned off to shut the output down by dropping the CS pin voltage below 0.68V. In this way, comparator C1 can be used for output on-off control.

As explained above, the CS pin can be used for soft-start, overload output shutdown, and output on-off control by varying the voltage. Further details on the above three major functions of the CS pin are given below.

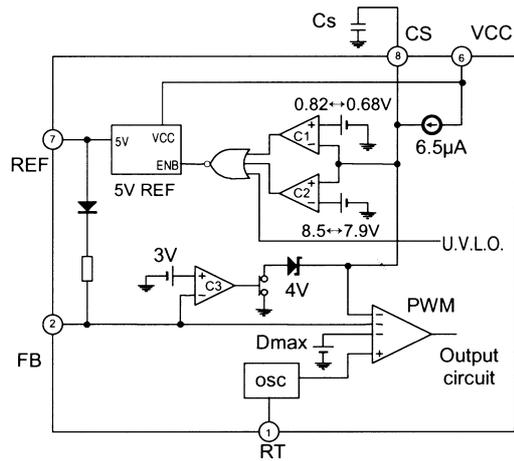
**4.1 Soft start function**

Figure 8 shows the soft start circuit. Figure 9 is a soft-start operation timing chart. The CS pin is connected to capacitor Cs. When the power is turned on, the constant current source (6.5µA) begins to charge the capacitor. As shown in the timing chart, the CS pin voltage rises slowly in accordance with the capacitor Cs charging current. The CS pin is also connected to the IC internal PWM comparator, which has such characteristics that the voltage is determined to output on the basis of the lowest of input voltages. The comparator output pulse slowly widens to cause a soft start as shown in the timing chart.

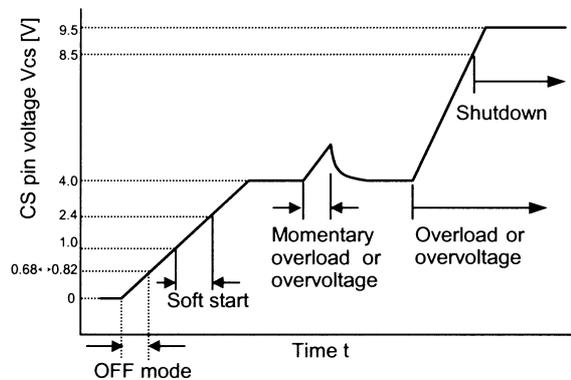
The soft start period can be approximately estimated by the period ts, from the time the IC is activated to the time the output pulse width widens to 30%. The period is given by the following equation:

$$t_s [\text{ms}] \approx 250 \times C_s \dots\dots\dots (3)$$

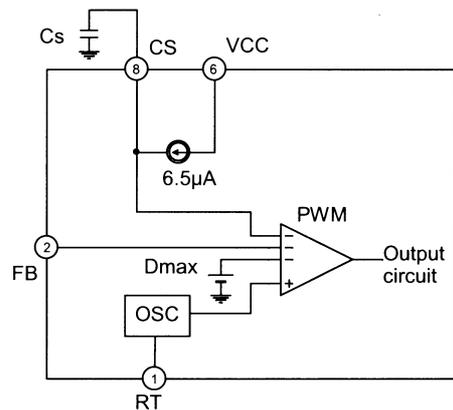
Cs : Soft start capacitor [µF]



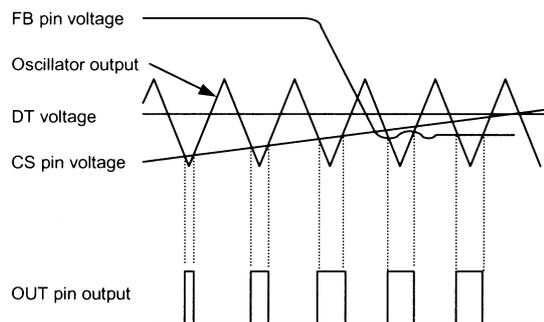
**Fig. 6 CS pin circuit**



**Fig. 7 CS pin waveform**



**Fig. 8 Soft-sart circuit**



**Fig. 9 Soft-sart timing chart**



**5. Overcurrent limiting circuit**

The overcurrent limiting circuit detects the peak value of every drain current pulse (pulse by pulse method) of the main switching MOSFET to limit the overcurrent. The detection threshold voltage is +0.235V for FA3641 or -0.168V for FA3647 with respect to the ground as shown in Figure 14.

The drain current of the MOSFET is converted to voltage by resistor  $R_s$  and fed to the IS pin of the IC. If the voltage exceeds the reference voltage +0.235V (FA3641) or -0.168V (FA3647) of comparator C4, comparator C4 works to set flip-flop output Q to high. The output is immediately turned off to shut off the current. Flip-flop output Q is reset on the next cycle to turn on the output again. This operation is repeated to limit the overcurrent.

If the overcurrent limiting circuit malfunctions due to noise, place an RC filter between the IS pin and MOSFET as shown in Figure 14. (See item 14 in "Design advice.")

Figure 15 is a timing chart that illustrates overcurrent-limiting operations.

**6. Vcc overvoltage protection circuit**

The IC contains a Vcc overvoltage protection circuit to protect the IC from damage by overvoltage. Figure 16 shows the overvoltage protection circuit. Figure 17 is a timing chart that illustrates overvoltage protection operations.

Overvoltage is detected if the supply voltage  $V_{cc}$  rises to 32V ( $I_{cc} = 13mA$ ) or more and current flows in the built-in zener diode. The output of comparator C5 then goes high and the constant current source (0.9mA) raises the CS pin voltage. When the CS pin voltage exceeds 8.5V, the output of comparator C2 goes high to turn off the 5V REF circuit. The IC then enters the latched mode and the IC output is put in the off (low voltage) state. When latched mode, the IC current consumption is 45 $\mu$ A (typ) ( $V_{cc} = 10V$ ). This current must be supplied through the startup resistor.

The overvoltage shutdown operation can be reset by lowering the supply voltage to below 9.0V or forcing the CS pin voltage below 7.9V.

(When you want to enable Vcc overvoltage shutdown at a desired voltage, see item 7 in "Design advice.")

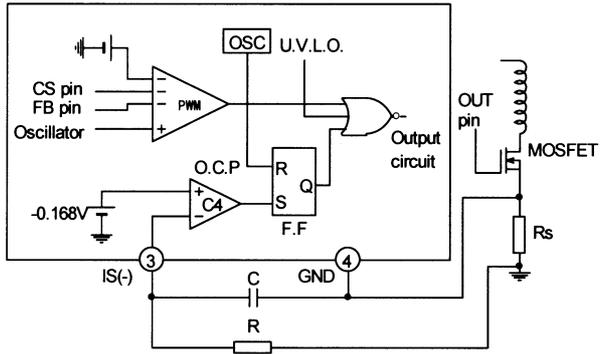
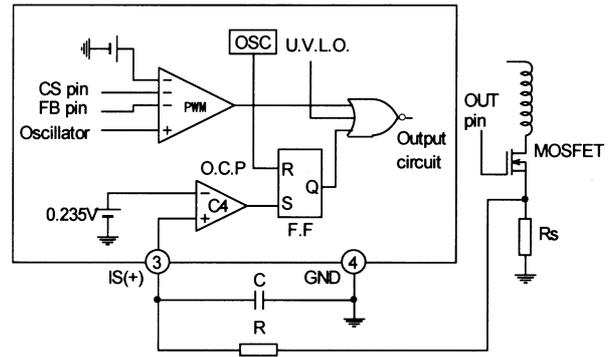


Fig. 14 Overcurrent limiting circuit

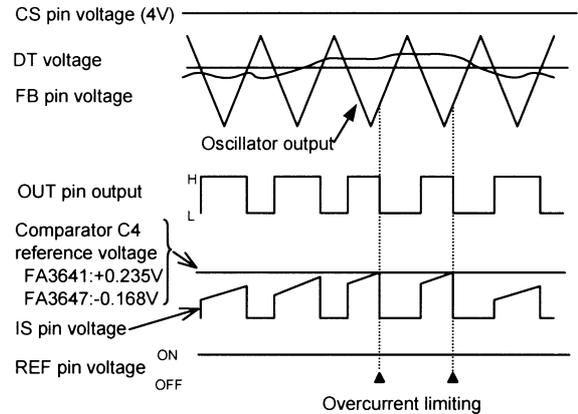


Fig. 15 Overcurrent timing chart

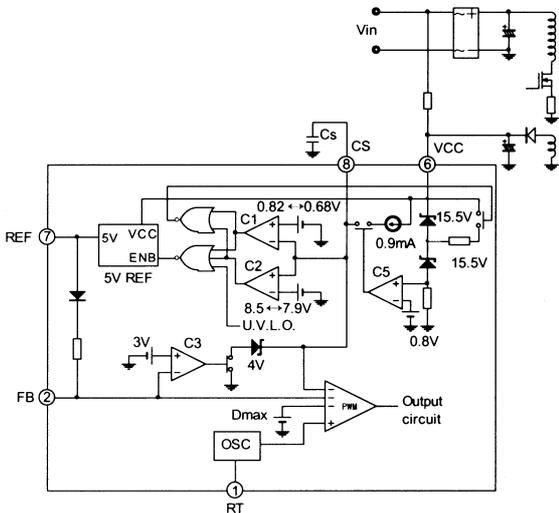


Fig. 16 Overvoltage shutdown circuit

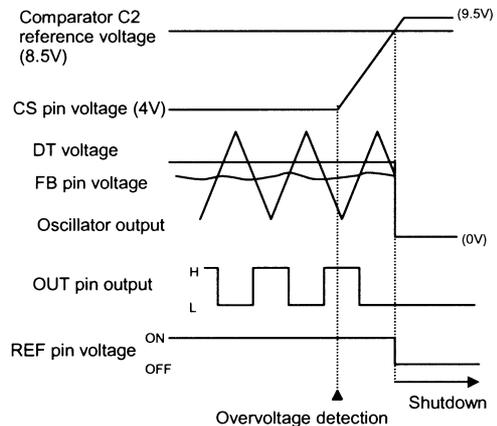


Fig. 17 Overvoltage shutdown timing chart

**7. Undervoltage lockout circuit (U.V.L.O.)**

The IC incorporates a circuit that prevents the IC from malfunctioning when the supply voltage drops. When the supply voltage is raised from 0V, the IC starts operation with Vcc = 16.5V (typ). If the supply voltage drops, the output is shut down when Vcc = 9.0V (typ). When the undervoltage lockout circuit operates, the outputs of the OUT and CS pins go low to reset the IC.

**8. Output circuit**

The IC contains a push-pull output stage and can directly drive the MOSFET. The maximum peak current of the output stage is a sink current of 1A and a source current of 0.5A. If the circuit operation stops when the undervoltage lockout circuit operates, the OUT pin voltage goes low to shut down the MOSFET.

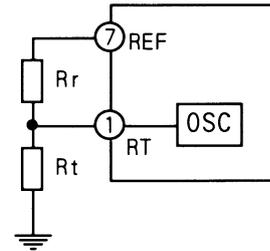


Fig. 18 Oscillator circuit

**■ Design advice**

**1. Externally setting the oscillation frequency in the light-load mode**

As explained in item 2 in “Description of each circuit,” the IC has a function that automatically lowers the oscillation frequency when the load is light, to reduce the loss of the power supply in standby mode. The oscillation frequency goes down to about 46% without adjustment by external circuit.

To further lower the frequency to below 46%, connect adjustment resistor Rr between the RT and REF pins as shown in Figure 18. Then the fixed frequency determined by Rt also falls. The relationship between the external resistance and oscillation frequency is outlined below:

$$Rt [k\Omega] \cong \frac{2.35}{3.35A - B} \quad Rr [k\Omega] \cong \frac{2.35}{A - B} \dots\dots\dots (5)$$

$$fo [kHz] \cong \frac{4880}{\frac{RtRr}{Rr - Rt} + 1.4} \quad fr [kHz] \cong \frac{2500}{\frac{RtRr}{Rr - 3.35Rt} + 6} \dots\dots (6)$$

- fo: Fixed frequency [kHz]
- fr: Minimum frequency in variable mode [kHz]
- Rt: Timing resistance [kΩ]
- Rr: Adjustment resistance [kΩ]

$$A = \frac{fo}{4880 - 1.4fo} \quad B = \frac{fr}{2500 - 6fr}$$

Select Rt and Rr so that the relationship between the two satisfies the following:

- Rt < 0.3 Rr ..... (7)
- Set the minimum frequency in light-load mode to 10 kHz or more.

Failure to keep the above relationship may disturb the operation.

Note that the above expressions determine approximate values. Note also that the minimum frequency in light-load mode depends on such conditions as the power supply efficiency. Therefore, check the operation using a practical circuit to make a final decision.

**Calculation example**

To set the fixed frequency fo = 100kHz and minimum frequency in light-load mode to fr = 20kHz, the following can be obtained from expressions (5).

$$Rt \cong 37.7 [k\Omega] \quad Rr \cong 185.1 [k\Omega]$$

Decrease Rr to permit the frequency to vary in a wider range.

**2. Deciding the startup circuit**

These ICs, which use CMOS process, consume less current, and therefore can use larger startup resistance than the conventional bipolar type of IC.

To decide the startup resistance, the following conditions must be satisfied:

- (a) The IC is started when the power is turned on.
- (b) The IC consumption current is supplied during latch mode operation to maintain the latch state.
- (c) The IC consumption current is supplied during the off state under the on/off function to maintain the off state.

However, these are the minimum conditions for using the IC. The startup time required for the power supply must also be decided on.

**2.1 Connecting a startup resistor before rectification (AC line)**

When the startup resistor is connected before rectification (AC line) as shown in Figure 19, the voltage applied to the startup resistor forms a half-wave rectified waveform of the AC input voltage.

Startup resistor R1 must satisfy the three equations shown below. Select a smaller-side value for R1 in consideration of the temperature characteristics.

- (a) To supply startup current 30μA at ON threshold voltage 17.5V (max.) of UVLO:

$$R1 [k\Omega] < \frac{\frac{\sqrt{2}}{\pi} \times Vac - 17.5}{0.03} \dots\dots\dots (8)$$

- (b) To supply IC consumption current 100μA (max.) (Vcc =10V) in latch mode:

$$R1 [k\Omega] < \frac{\frac{\sqrt{2}}{\pi} \times Vac - 10}{0.1} \dots\dots\dots (9)$$

- (c) To supply IC consumption current 200μA (max.) (Vcc =17V) in the off state under the on/off function:

$$R1 [k\Omega] < \frac{\frac{\sqrt{2}}{\pi} \times Vac - 17}{0.2} \dots\dots\dots (10)$$

R1: Startup resistance [kΩ]

Vac: Effective value of AC input voltage [V]

If neither the latch mode operation nor the on/off functions are used, only the expression in (8) needs to be satisfied. In this method, the supply current to the IC via the start-up resistor is stopped when AC input is shut down. Therefore, after latch mode operation, shutting the AC input down resets the latch mode in a very short period of time.

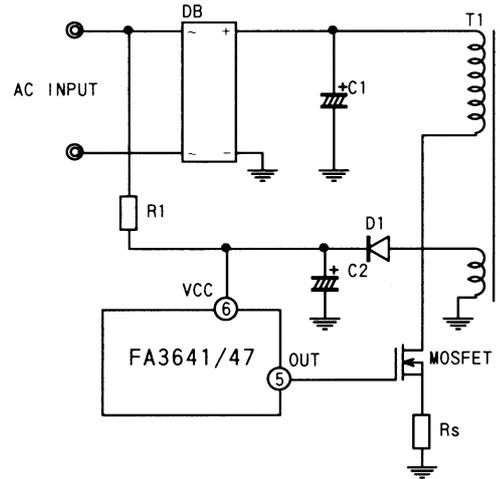
**2.2 Connecting the startup resistor after rectification (DC line)**

When the startup resistor is connected after rectification (DC line) as shown in Figure 20, the voltage applied to the startup resistor becomes the peak value of the AC input voltage.

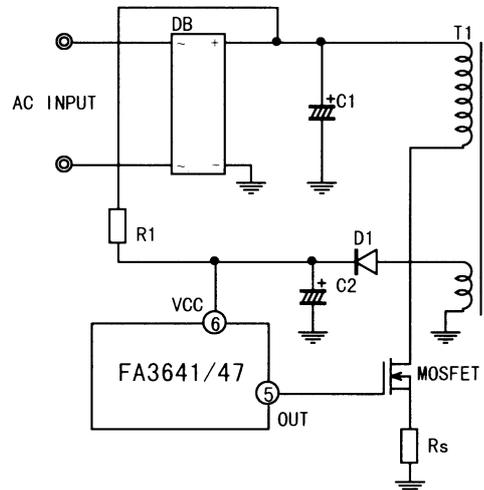
Startup resistor R1 must satisfy the three equations shown below. Select a smaller-side value for R1 in consideration of temperature characteristics.

- (a) To supply startup current 30μA at ON threshold voltage 17.5V (max.) of UVLO:

$$R1 [k\Omega] < \frac{\sqrt{2} \times Vac - 17.5}{0.03} \dots\dots\dots (11)$$



**Fig. 19 Startup circuit (1)**



**Fig. 20 Startup circuit (2)**

(b) To supply IC consumption current 100µA (max.) (Vcc = 10V) in latch mode:

$$R1 [k\Omega] < \frac{\sqrt{2} \times V_{ac} - 10}{0.1} \dots\dots\dots (12)$$

(c) To supply IC consumption current 200µA (max.) (Vcc = 17V) in the off state under the on/off function:

$$R1 [k\Omega] < \frac{\sqrt{2} \times V_{ac} - 17}{0.2} \dots\dots\dots (13)$$

R1: Startup resistance [kΩ]  
 Vac: Effective value of AC input voltage [V]

If neither the latch nor the on/off functions are used, only the expression in (11) needs to be satisfied. In this method, after latch mode operation, smoothing capacitor C1 in the main circuit supplies current to the IC via the startup resistor even if the AC input is shut down. Therefore, some time must elapse before the latch mode is reset.

**3. Determining the Vcc capacitor value**

To properly start the power supply, a certain value is required for the capacitor connected to the VCC pin. Figure 21 shows the Vcc voltage at start-up when a proper value is given to the capacitor.

When the input power is turned on, the capacitor connected to the VCC pin is charged via the startup resistor and the voltage increases. The IC is then in standby state and almost no current is consumed. (Icc < 2µA)

Thereafter, Vcc reaches the ON threshold voltage of UVLO and the IC begins operation.

When the IC begins operation to make output, the IC operates based on the voltage from the auxiliary winding. When the IC is just starting up, however, it takes time for the voltage from the auxiliary winding to rise enough, and Vcc drops during this period.

Determine the Vcc capacitor value so that Vcc will not drop down to the OFF threshold voltage of UVLO during this period. If the Vcc capacitor value is too small, Vcc will drop to the OFF threshold voltage of UVLO before the auxiliary winding voltage rises enough. If so, Vcc repeatedly goes up and down between the UVLO threshold voltages, and the power supply cannot start up. (Figure 22)

**4. Shortening the startup period**

Increasing the resistance of the startup resistor to reduce loss prolongs the startup period. Figure 23 shows a circuit for shortening the startup period. The C2 capacitance is decreased to shorten the startup period and, after the IC starts up, power is supplied from C3.

**5. Setting soft start period and OFF latch delay independently**

Figure 24 shows a circuit for setting the soft start period and OFF latch delay independently. In this circuit, capacitance CS determines the soft start period, and capacitance CL determines the OFF latch delay.

If the overload shutdown or overvoltage shutdown functions raise the CS pin voltage to around 5V, zener diode Zn becomes conductive to charge capacitor CL. The OFF latch delay can be thus prolonged by capacitance CL.

When the capacitor value is adequate

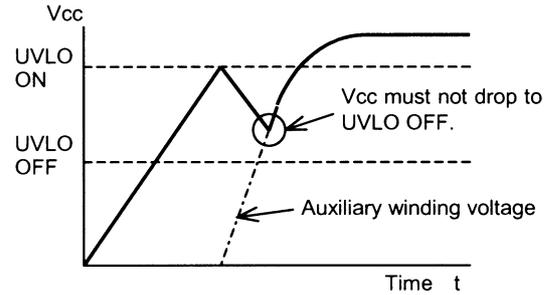


Fig. 21 Vcc voltage at startup with an adequate capacitor

When the capacitor value is inadequate

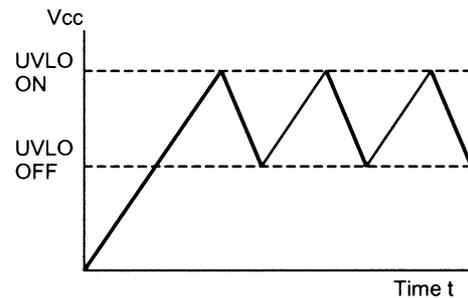


Fig. 22 Vcc voltage at startup with an inadequate capacitor

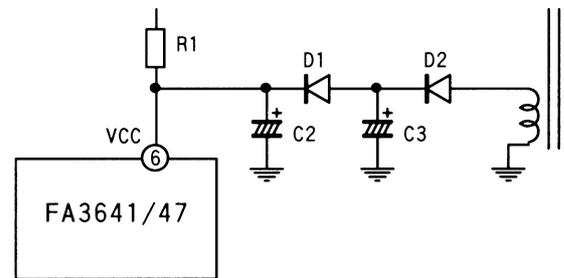


Fig. 23 Startup circuit (3)

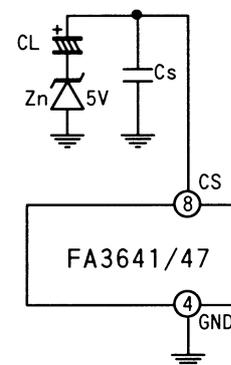


Fig. 24 Independent setting of soft start period and OFF latch delay

**6. Overvoltage protection using the VCC pin**

These ICs contain an overvoltage protection function detecting the Vcc voltage using internal ZD (See item 6 in "Description of each circuit"). If Vcc voltage exceed about 32V, the current of 13mA flows through the internal ZD and the overvoltage protection function operates.

After this protection function operates, the IC continues to consume the large current if high voltage continues to be applied to the Vcc pin. Mind that total IC loss does not exceed the rating.

If the voltage source applied to Vcc pin has relatively high impedance and cannot supply the current of 13mA, overvoltage protection function does not operate. But the internal ZD maintains the Vcc voltage 32V or less and protects the IC.

**7. Overvoltage protection using CS pin**

These ICs contain the overvoltage protection function detecting Vcc voltage. However, the threshold voltage is fixed. Adding a circuit to CS pin enables the overvoltage protection detecting desired voltage.

**7.1 Detecting on secondary side**

Figure 25 shows the overvoltage shutdown circuit based on the signal from the secondary side. The optocoupler output transistor is connected between the CS and Vcc pins. When the output voltage is put in the overvoltage state, the optocoupler output transistor goes on to raise the CS pin voltage via resistor R2. When the CS pin voltage exceeds the reference voltage (8.5V) of comparator C2, the output of the comparator C2 goes high to turn off the 5V REF circuit. Accordingly, the IC enters the OFF latch mode and shuts the output down. The IC consumes current 45µA (typ) (Vcc = 10V) in latch mode. This current must be supplied via startup resistor R1.

The overvoltage protection circuit can be reset by lowering the supply voltage Vcc to below 9.0V or forcing the CS pin voltage below 7.9V.

In normal operation, the CS pin voltage is clamped by the 4V zener diode with maximum sink current 50µA. Therefore, to raise the CS pin voltage to 8.5V or more, 50µA or a higher current needs to be supplied from the optocoupler. Set the current input to the CS pin to 1mA or less.

**7.2 Detecting on primary side (detecting Vcc voltage)**

To attain overvoltage protection, the CS pin voltage is forcibly raised from outside the IC until it exceeds the reference voltage (8.5V) of the internal comparator C2. When the reference voltage is exceeded, the IC enters latch mode and shuts the output down. Connect a zener diode (ZD) and resistor between the Vcc and CS pins as shown in Figure 26. When the Vcc voltage exceeds about ZD voltage + 8.5V, the ICs enter the OFF latch mode and shut the output down. If Vcc remains high even after shutdown and current is input to the CS pin, set the current to 1mA or lower.

Set the zener voltage of the ZD connected to the CS pin higher than the UVLO ON threshold voltage. Startup is disabled below this voltage.

Figure 27 shows another circuit for enabling latch mode shutdown by detecting a desired Vcc voltage using the CS pin. In this circuit, overvoltage shutdown works when the Vcc voltage is about the same as the ZD voltage. For this circuit also, use a ZD voltage higher than the UVLO ON threshold voltage. Set the current flowing into the CS pin to 1mA or lower.

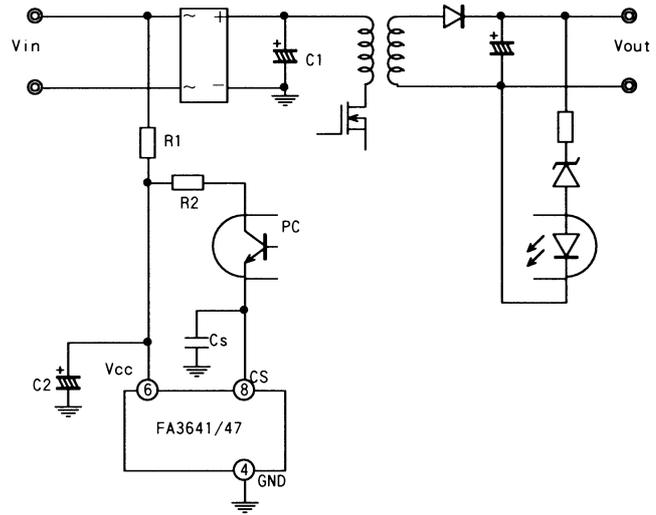


Fig. 25 Overvoltage shutdown circuit (1)

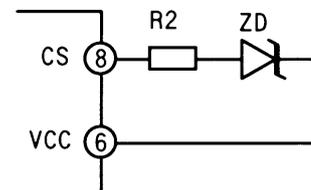


Fig. 26 Overvoltage shutdown circuit (2)

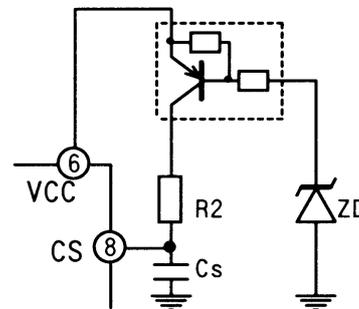


Fig. 27 Overvoltage shutdown circuit (3)

**8. Feedback pin circuit**

Figure 28 gives an example of connection in which a feedback signal is input to the FB pin.

If this circuit causes power supply instability, connect R3 and C4 as shown in Figure 28 to decrease the frequency gain. Set R3 between several tens of ohms to several kilohms and C4 between several thousand picofarads to one microfarad. Be especially careful in light load mode, in which the frequency drops, thereby increasing the probability of power supply instability being triggered.

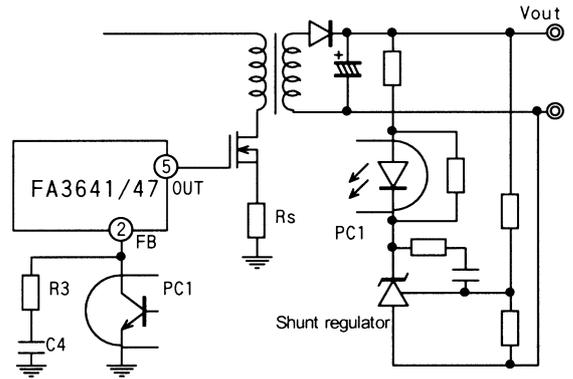


Fig. 28 FB pin circuit

**9. REF characteristics**

If noise is applied to the VCC pin from the outside, it may appear at the REF pin without attenuation depending on the noise frequency. The noise causes no problems in normal IC operation, but must be taken into consideration when the REF voltage is used for an external circuit. If the noise appearing at the REF pin causes any problems, use the REF pin as shown in Figure 29.

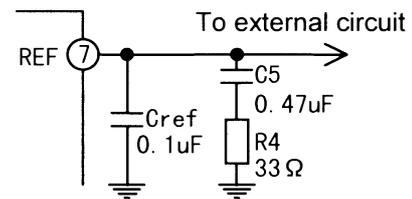


Fig. 29 REF pin circuit

**10. Simple voltage control on the primary side**

In a flyback type power supply, the output voltages of the power supply and auxiliary winding are almost proportional to the number of winding turns of the transformer. This characteristic can be used in the circuit shown in Figure 30, where the output voltage can easily be made constant by detecting the voltage of the auxiliary winding voltage.

However, this is an easy output voltage control method, and the output voltage precision and regulation are therefore not as good.

To reduce output pulse width completely to 0%, the FB pin voltage must fall below 0.95V and R5 must be set below about 960Ω from the characteristics of the FB pin voltage and source current. When using this method, also keep in mind the characteristics of REF in item 9.

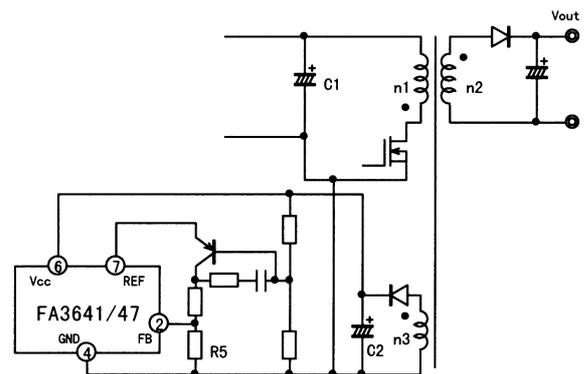


Fig. 30 Simple voltage control circuit

**11. Disabling the overload shutdown function**

As shown in Figure 31, connect a 8.2kΩ resistor R6 between the FB pin and the ground. The FB pin voltage then does not rise sufficiently high to reach the shutdown threshold voltage when an overload occurs so that IC does not enter OFF latch mode. Even with this connection, the overvoltage shutdown function is available.

Since resistor R6 limits the upper voltage of the FB pin, the maximum duty cycle may be limited to about 65%, if a 5% precision resistor is used. To not limit the maximum duty cycle, use a 2% or better-precision resistor for R6.

**12. Polarities for overcurrent detecting and their characteristics**

The FA3641 uses positive polarity detection for overcurrent limiting (number 3 pin of IS pin) and the FA3647 uses negative polarity detection. The characteristics of positive and negative polarity detection are summarized below. Select one in accordance with the circuit used. (See item 5 in "Description of each circuit.")

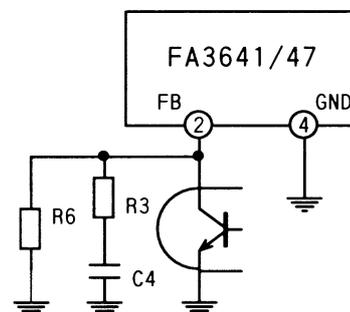


Fig. 31 Disabling overload shutdown function

**Positive detection (FA3641)**

- Wiring is easy because the ground can be shared by the main circuit and IC peripherals.
- It is easy to correct the overload detecting current, which is used to detect overload, against the input voltage.

**Negative detection (FA3647)**

- The MOSFET drive current does not flow to the current detection resistor and therefore it hardly affects overcurrent detection.

**13. Correcting overload detection current (FA3641 only)**

If the power supply output is overloaded, the IC overcurrent limiting function restricts the output power and the overload shutdown function stops the IC. The output current when an overload occurs varies depending on the input voltage; the higher the input voltage, the more the overload detection current may increase.

If any problems occur as a result of the appearance of this symptom, connect resistor R8 between current detection resistor R<sub>s</sub> and the IS (+) pin and add resistor R7 for correction as shown in Figure 32. The standard resistance of R8 is several hundred ohms, and that of R7 is from several hundred kilohms to several megohms.

Note that the above correction slightly lowers the output current when overload even where the input voltage is low. This correction is available only for the FA3641 that uses positive polarity for overcurrent detection.

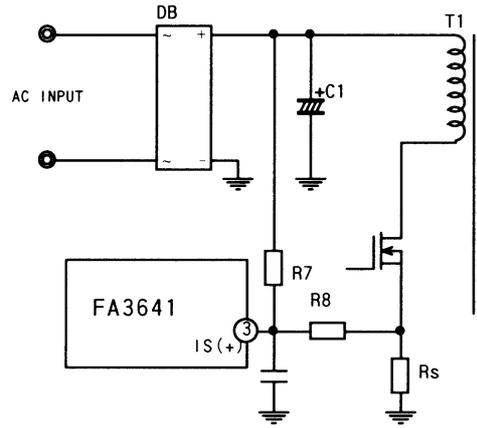


Fig. 32 Correcting overload detecting current circuit

**14. Preventing malfunction caused by noise**

The IS pin for overcurrent limiting function detects the MOSFET current converted to the voltage. The parasitic capacitor and inductor of the MOSFET, transformer, wiring, etc. cause a noise in switching operation. If this switching noise causes a malfunction of overcurrent limiting function, insert the RC filter into IS pin as shown in Figure 14.

Also, connect a noise prevention capacitor (0.1μF or more) to the REF pin that outputs the reference voltage for each component.

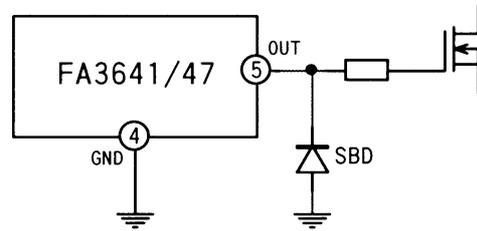


Fig. 33 Protection of OUT pin against the negative voltage

**15. Preventing malfunction caused by negative voltage applied to a pin**

When large negative voltage is applied to each IC pin, a parasitic element in the IC may operate and cause malfunction. Be careful not to allow the voltage applied to each pin to drop below -0.3V.

Especially for the OUT pin, voltage oscillation caused after the MOSFET turns off may be applied to the OUT pin via the parasitic capacitance of the MOSFET, causing the negative voltage to be applied to the OUT pin. If the voltage falls below -0.3V, add a Schottky diode between the OUT pin and the ground. The forward voltage of the Schottky diode can suppress the voltage applied to the OUT pin.

Use the low forward voltage of the Schottky diode. Similarly, be careful not to cause the voltages at other pins to fall below -0.3V.

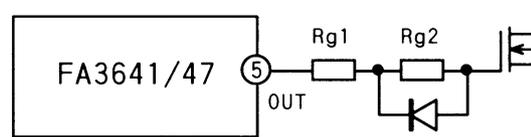


Fig. 34 Gate circuit

**16. Gate circuit configuration**

To adjust switching speeds or prevent oscillation at gate terminals, resistors are normally inserted between the power MOSFET gate terminal to be driven and the OUT pin of the IC. You may prefer to decide on the drive current independently, to turn the MOSFET on and off. If so, connect the MOSFET gate terminal to the OUT pin of the IC as shown in Figure 34.

In the circuit shown in Figure 34, Rg1 and Rg2 restrict the current when the MOSFET is turned on, and only Rg1 restricts the current when it is turned off.

**17. Loss calculation**

IC loss must be confirmed to use the IC within the ratings. Since it is hard to directly measure IC loss, some examples of calculating approximate IC loss are given below.

**17.1 Calculation example 1**

Suppose the supply voltage is  $V_{cc}$ , IC current consumption is  $I_{ccop}$ , the total gate charge of the power MOSFET is  $Q_g$ , and the switching frequency is  $f_{sw}$ . Total IC loss  $P_d$  can be calculated by:

$$P_d = V_{cc} \times (I_{ccop} + Q_g \times f_{sw}) \dots\dots\dots (14)$$

This expression calculates an approximate value of  $P_d$ , which is normally a little larger than the actual loss. Since various conditions such as temperature characteristics apply, thoroughly verify the appropriateness of the calculation under all applicable conditions.

**Example:**

When  $V_{cc} = 18V$ ,  $I_{ccop} = 2.5mA$  (max.) is obtained from the specifications. Suppose  $Q_g = 80nC$  and  $f_{sw} = 100kHz$ .

$$P_d = 18V \times (2.5mA + 80nC \times 100kHz) = 189mW$$

**17.2 Calculation example 2**

The IC loss consists of the loss caused by operation of the control circuit and the loss caused at the output circuit to drive the power MOSFET.

**(1) Loss at the control circuit**

The loss caused by operation of the IC control circuit is calculated by the supply voltage and IC current consumption. When the supply voltage is  $V_{cc}$  and IC current consumption is  $I_{ccop}$ , loss  $P_{op}$  at the control circuit is:

$$P_{op} = V_{cc} \times I_{ccop} \dots\dots\dots (15)$$

**Example:**

When  $V_{cc} = 18$ ,  $I_{ccop} = 1.9mA$  (typ) is obtained from the specifications. The typical IC loss is given by:

$$P_{op} = 18V \times 1.9mA = 34.2mW$$

**(2) Loss at the output circuit**

The output circuit of the IC is a MOSFET push-pull circuit. When the ON resistances of MOSFETs making up the output circuit are  $R_{on}$  and  $R_{off}$ , the resistances can be determined as shown below based on  $V_{cc} = 18V$  and  $T_j = 25^\circ C$  obtained from the output characteristics included in the specifications:

$$R_{on} = 15\Omega \text{ (typ)}$$

$$R_{off} = 7\Omega \text{ (typ)}$$

When the total gate charge of the power MOSFET is  $Q_g$ , the switching frequency is  $f_{sw}$ , the supply voltage is  $V_{cc}$ , and gate resistance is  $R_g$ , the loss caused at the IC output circuit is given by:

$$P_{dr} = \frac{1}{2} \times V_{cc} \times Q_g \times f_{sw} \times \left( \frac{R_{on}}{R_g + R_{on}} + \frac{R_{off}}{R_g + R_{off}} \right) \dots\dots (16)$$

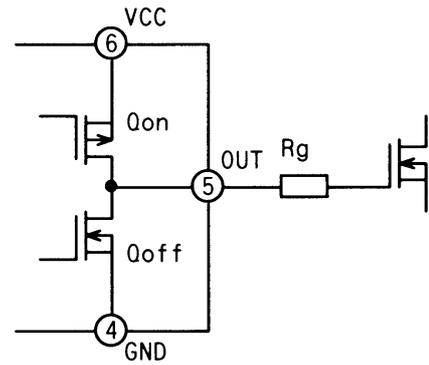


Fig. 35 Output stage

## FA3641P(N), FA3647P(N)

When gate resistance differs between ON and OFF as shown in Figure 36, the loss is given by:

$$P_{dr} = \frac{1}{2} \times V_{cc} \times Q_g \times f_{sw} \times \left( \frac{R_{on}}{R_{g1} + R_{g2} + R_{on}} + \frac{R_{off}}{R_{g1} + R_{off}} \right) \dots (17)$$

**Example:**

When  $V_{cc} = 18V$ ,  $Q_g = 80nC$ ,  $f_{sw} = 100kHz$ , and  $R_g = 10\Omega$ , the typical IC loss is given by:

$$P_{dr} = \frac{1}{2} \times 18V \times 80nC \times 100kHz \times \left( \frac{15\Omega}{10\Omega + 15\Omega} + \frac{7\Omega}{10\Omega + 7\Omega} \right) = 72.8mW$$

**(3) Total loss**

The total loss ( $P_d$ ) of the IC is the sum of the control circuit loss ( $P_{op}$ ) and the output circuit loss ( $P_{dr}$ ) calculated previously:

$$P_d = P_{op} + P_{dr} \dots (18)$$

**Example:**

The standard IC loss under the conditions used in (1) and (2) above are:

$$P_d = P_{op} + P_{dr} = 34.2mW + 72.8mW = 107mW$$

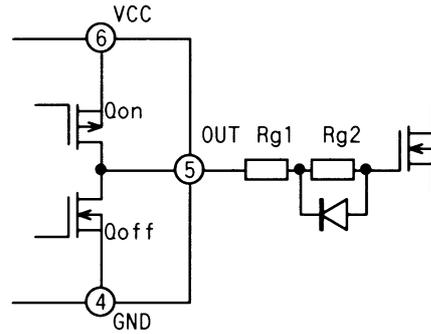
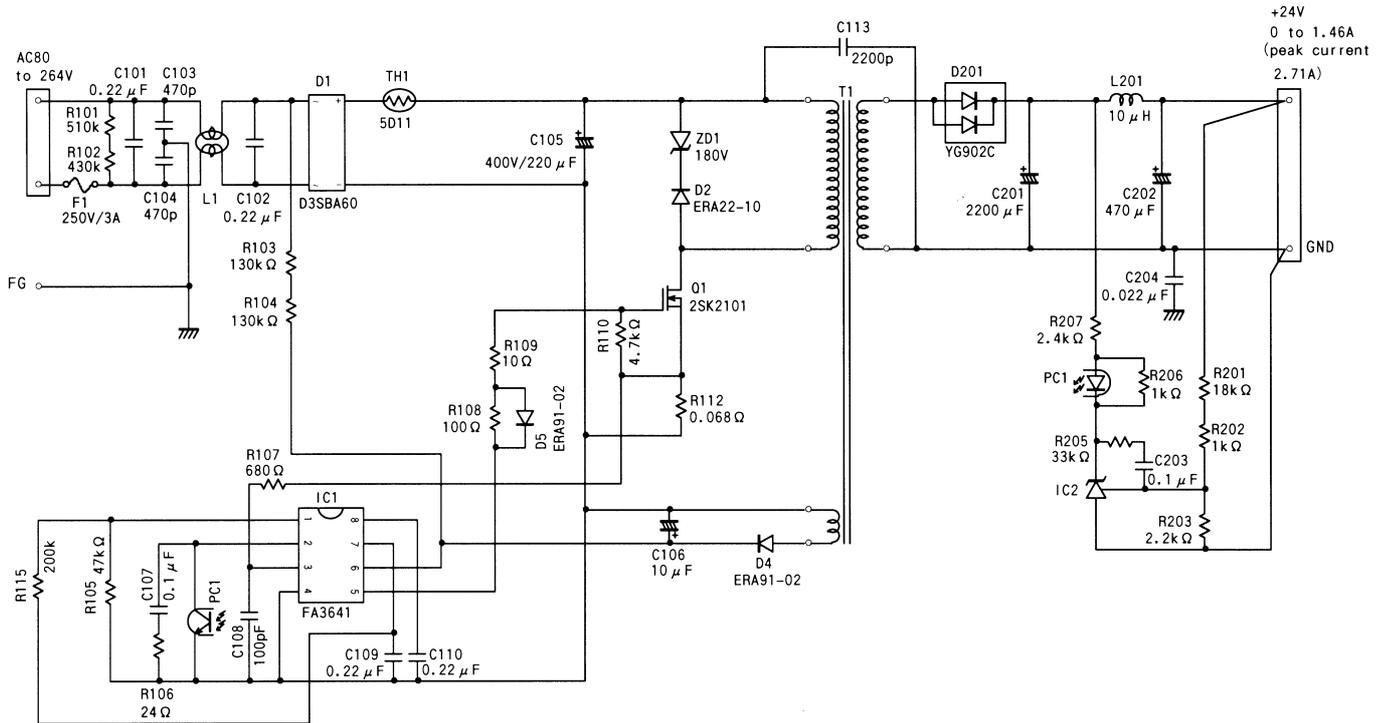


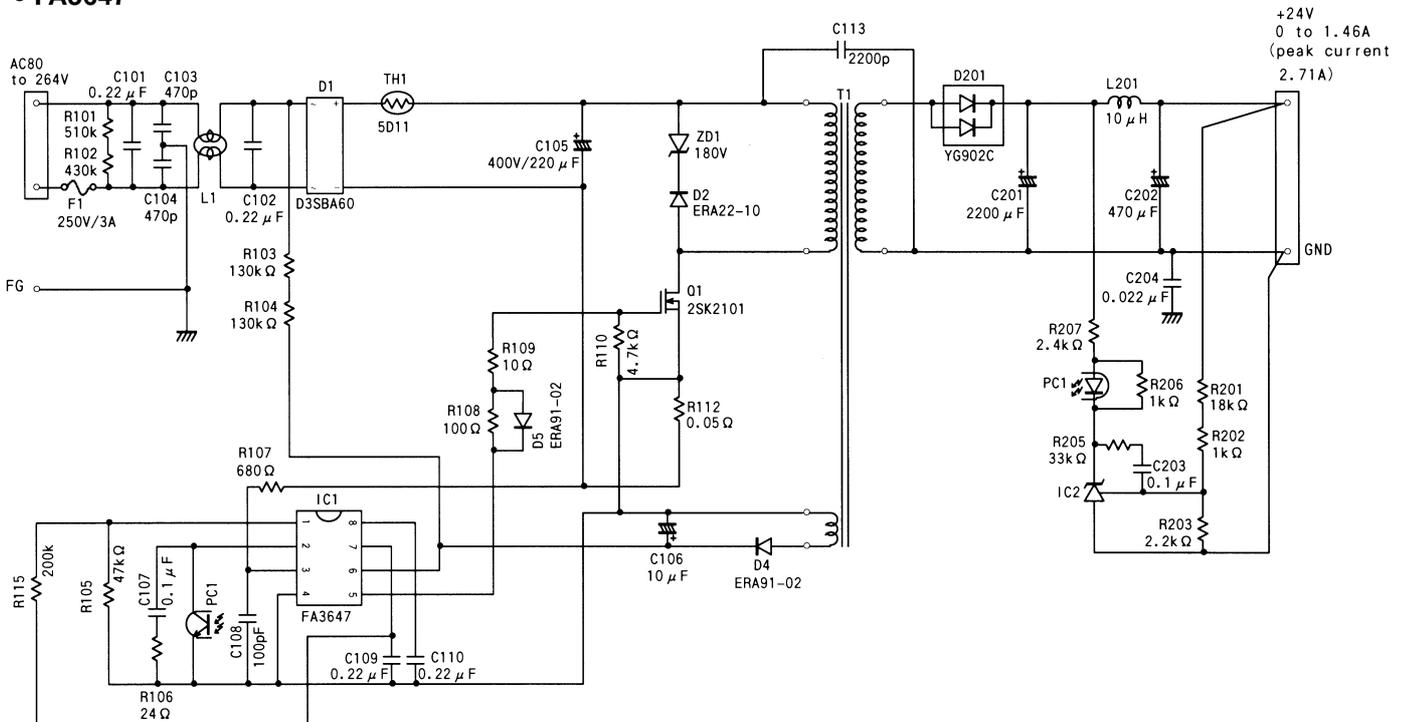
Fig. 36 Gate circuit

■ Application circuit

● FA3641



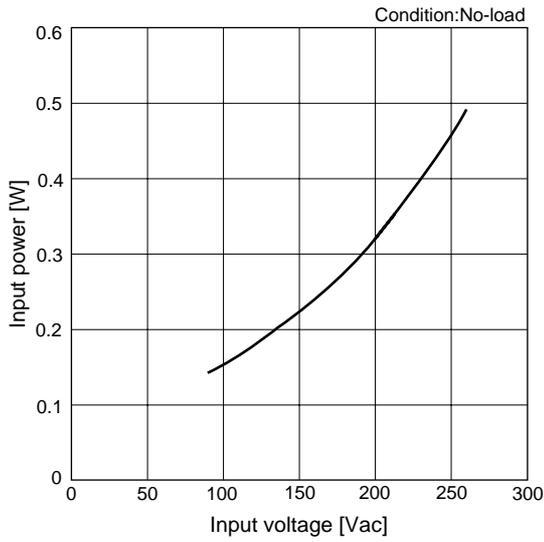
● FA3647



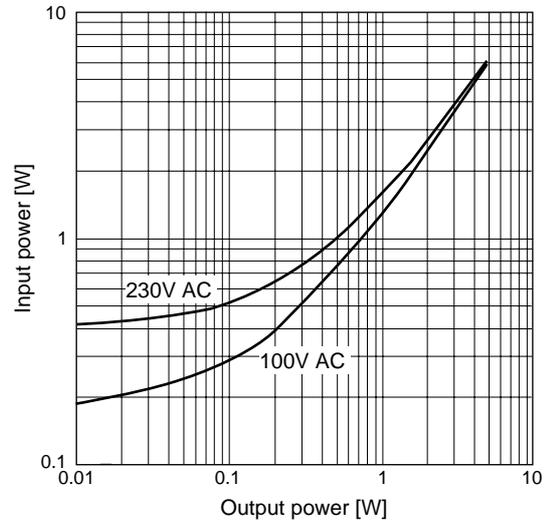
Parts tolerances characteristics are not defined in the circuit design sample shown above. When designing an actual circuit for a product, you must determine parts tolerances and characteristics for safe and economical operation.

■ Electrical characteristics of application circuit

Input power vs. input voltage



Input power vs. output power



Oscillation frequency vs. output power

